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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,853	10/28/2003	Krishna K. Pappu	03-0128 81615	6739
7590	11/14/2006			EXAMINER PARIHAR, SUCHIN
Leo J. Peters LSI Logic Corporation MS D-106 1551 McCarthy Blvd. Milpitas, CA 95035			ART UNIT 2825	PAPER NUMBER
DATE MAILED: 11/14/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,853	PAPPU ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 08 September 2006.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-18 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application
6) Other: _____

DETAILED ACTION

This FINAL office action is in response to application 10/695,853, amendment filed 9/8/2006.

Applicant's arguments filed 9/8/2006 have been fully considered but they are not persuasive. The applicable rejections from the prior office action are incorporated herein.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 1 and 10 are rejected under 35 U.S.C. 112, second paragraph**, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: prior to step (c), determining whether a cell or cells belongs to one of **the common signal domains**. More specifically, since step (c) involves "selecting a cell that belongs to one of the common signal domains", those with ordinary skill in the art would not know how to select a cell that belongs to one of the common signal domains without first determining whether that selected cell, does in fact, belong to one of the common signal domains.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang (5,828,579) in view of Nadeau-Dostie et al. (6,457,161).**
5. With respect to claims 1 and 10, Beausang teaches a method of grouping cells for scan testing, which includes teaching a computer program/computer program product (description of CAD & computer system, Col 6, lines 1-42), comprising the steps of:
 - receiving as input a representation of an integrated circuit design (database [netlist] 210 that defines an IC design, acting as input to the system 205 of Figure 1B, Col 6, lines 53-55);
 - initializing (i.e. constructing) a corresponding list of cells for each of a plurality of common signal domains in the integrated circuit design (constructing scan chains [i.e. lists] being of a common clock domain, Col 4, lines 5-15), each corresponding list of cells created as an empty list (set of chains that are compatible with a particular clock domain may start out as empty, as suggested by 320 of Figure 2A);
 - selecting (i.e. accessing) a cell that belongs to one of the common signal domains and that is not included in a corresponding list of cells for any of the common signal domains (accessing segments [i.e. cell] that have not been assigned to a scan chain [list], Col 26, lines 60-65 & Col 27, lines 1-5); and
 - inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15).

Beausang does not specifically teach tracing steps that involve tracing a net to/from an input port of each cell connected to a signal driver.

However, Nadeau-Dostie et al. teaches a method/computer-tool for representing a circuit that involves tracing to/from an input port of each cell connected to a signal driver to identify the cells being connected (Col 7 line 67 to Col 8 line 57, i.e. signal tracing module).

It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the teachings of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain of the method/system of Beausang.

6. With respect to claims 2 and 11, Beausang in view of Nadeau-Dostie et al. teaches all the elements of claims 1 and 10, from which the respective claims depend, as described above. Beausang also teaches repeating steps (c), (d), (e), (f) and (g) until every cell belonging to the common signal domain associated with the signal driver has been inserted in a corresponding list of cells for the common signal domain, (accessing all segments [i.e. cells] that have not already been assigned to a scan chain and partitions the segments by clock domain).

7. With respect to claims 3 and 12, Beausang in view of Nadeau-Dostie et al. teaches all the elements of claims 2 and 11 respectively, from which the respective claims depend, as described above. Beausang also teaches generating as output a

corresponding list of cells for a common signal domain in the integrated circuit design (generating as output a compiler generated script file which is a complete specification of the scan configuration, Col 10, lines 50-55, also see the figure in Col 10 indicating “scan chain 1” and “scan chain 2” and the cells they each contain).

8. With respect to claims 4 and 13, Beausang in view of Nadeau-Dostie teaches all the elements of claims 1 and 10 respectively. Beausang teaches: wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (during scan chain [i.e. list] construction, scan element name is included for each element, Col 16, lines 15-20, also see Col 10, lines 10-15).

9. With respect to claims 5 and 14, Beausang in view of Nadeau-Dostie teaches all the elements of claims 1 and 10, from which the respective claims depend, as discussed above. Beausang also teaches performing steps (b), (c), (d), (e), (f) and (g) for cells that are flip-flops in a scan chain (flip-flop is an example of a user defined segment, Col 14, lines 10-15).

10. With respect to claims 6 and 15, Beausang in view of Nadeau-Dostie teaches all the elements of claims 5 and 14, from which the claims depend respectively. Beausang teaches: performing steps (b), (c), (d), (f) and (g) for a common signal domain that is a scan clock domain (scan chains being of a common clock domain, Col 4, lines 1-15).

11. With respect to claims 7 and 16, Beausang in view of Nadeau-Dostie teaches all the elements of claims 6 and 15, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for a net that is a clock net.

However, Nadeau-Dostie teaches: performing steps (d), (e), (f), and (g) for a net that is a clock net (tracing backward from the clock input port of the latch to a clock source, wherein the connection between the clock input port and the clock source is considered a "clock net", Col 8, lines 1-15).

12. With respect to claims 8 and 17, Beausang in view of Nadeau-Dostie teaches all the elements of claims 7 and 16, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for an input port that is a clock port. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for an input port that is a clock port (clock input port of a latch, Col 8, lines 10-15).

13. With respect to claims 9 and 18, Beausang in view of Nadeau-Dostie teaches all the elements of claims 8 and 17, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for a signal driver that is a clock driver. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for a signal driver that is a clock driver (clock buffer 38 driven by a clock phase PH2 [i.e. driver], Col 4, lines 35-40).

Response to Arguments

14. Applicant's arguments filed 9/8/2006 have been fully considered but they are not persuasive.

15. Applicant asserts that because the scan chains in Beausang cited by the rejection are not empty scan chains, Beausang does not teach or suggest the claimed initialized corresponding list of cells for each common signal domain in which each

Art Unit: 2825

corresponding list of cells is created as an empty list. Examiner disagrees with this assertion.

16. Examiner points out that Beausang teaches: initializing a corresponding list (getting [retrieving] the set of chains compatible with the domain [i.e. chains of circuit blocks with same clock domain] which may start out empty as suggested by 320 of Figure 2A) of cells for each of a plurality of common signal domains in the integrated circuit design, each corresponding list of cells is created as an empty list (sets [i.e. lists] which may start out empty as suggested by 320 of Figure 2A).

17. Applicant asserts that Beausang does not teach or suggest selecting a cell belonging to one of the common signal domains that is not included in a corresponding list of cells for any of the common signal domains. Examiner disagrees with this assertion.

18. Examiner points out that Beausang teaches: selecting a cell that belongs to one of the common signal domains (accessing [i.e. selecting] a plurality of segments within the IC design including a member list of sequentially coupled [i.e. same domain] scan cells, Col 3 line 64 to Col 4 lines 1-6) and that is not included in a corresponding list of cells (i.e. that have not been assigned to a scan chain, Col 26, lines 60-65) for any of the common signal domains (i.e. first and second scan chains being each of a common signal domain, Col 4, lines 5-15).

19. Applicant asserts that Beausang does not teach or suggest inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver. Examiner disagrees with this assertion.

20. Examiner points out that Beausang teaches inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent

Art Unit: 2825

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PRIMARY EXAMINER

